REMARKS

Claims 1-25 are pending in the present application. The Examiner has rejected claims 1-7, 9-13, and 15-25 and objected to claims 8 and 14. Further, the Examiner has objected to the drawings and the specification of the applications. Applicants have amended the drawings and specification as indicated by the Examiner. Further, Applicants have amended claims 1 and 19 to clarify the invention and claims 8 and 14 as suggested by the Examiner. No new matter has been added by these amendments.

Drawings

The Examiner has objected to the drawings. In particular, the Examiner has indicated that Figures 1-4 should be labeled with the legend --Prior Art-- "because only that which is old is illustrated." Further, the Examiner has indicated that Figure 1 includes a reference sign, sign "24a," that was not mentioned in the description. Also, the Examiner has indicated that the description describes a reference number 34 that is not included in the Figures.

As indicated above, Figures 1-4 have been amended to include the legend --Prior Art--. Further, Figure 2 has been amended to include indication of element "34." The reference to element 24a of Figure 1 is included in the specification on line 6 of page 20; therefore, no amendment to Figure 1 with respect to the element "24a" is made.

Further, replacement sheets of all Figures that include the amendments made herein are included with this Amendment. Applicants, then, request that the Examiner remove the objections to the drawings.

Specification

The Examiner has objected to the specification because the abstract exceeds the range of 50 to 150 words. Also, the related application patent number should be included.

As suggested by the Examiner, the application has been reviewed and amendments have been made to correct typographical errors. The current abstract has been moved to the beginning of the Detailed Description and a new abstract has been added. Further, the specification has been amended such that the identification of the related application by application serial number has been made.

Therefore, Applicants request that the Examiner remove the objections to the specification.

Rejections under 35 USC § 102

The Examiner has rejected claims 1, 9, 15, and 19 under 35 U.S.C. § 102(b) as being anticipated by Caldara et al. (U.S. 6,141,346). Applicants herein traverse these rejections.

Caldara, however, does not teach several of the limitations of claims 1, 9, 15, and 19 as is suggested by the Examiner. With respect to claim 1, for example, Caldara does not teach "generating a multicast master entry in said connection table, said multicast master entry holding address locations at which multicast ATM cells are stored, said multicast master entry including a limit field and a count field," as is recited in claim 1. The examiner identifies the from switch port processor (FSPP) 16 shown in Figure 1 of Caldara as teaching this element. However, as taught in Caldara, "[t]he FSPP receives cells from the switch fabric and transmits those cells onto output links." (Caldara, col. 2, lines 57-59). Therefore, nowhere does Caldara teach that the FSPP includes "generating a multicast master entry in said connection table, said multicast master entry holding address locations at which multicast ATM cells are stored, said multicast master entry including a limit field and a count field," as is recited in claim 1.

Further, the Examiner indicates that the "connection table" recited in claim 1 is identified as the switch allocation table ("SAT") 20 shown in Figure 1. Even if that were the case, Caldara does not teach that the FSPP (identified by the Examiner as the "multicast master entry") is "in said connection table," as is recited in claim 1. Instead, Caldara teaches that the SAT and FSPP are two very separate elements. The SAT "manages bandwidth allocation and delay" and is located in the to switch port processor ("TSPP") (Caldara, col. 4, lines 7-10). In particular, Caldara teaches that "[e]ach SAT 20 includes a plurality of sequentially ordered cell time slots 50 and a pointer 52 which is directed to one of the slots." (Caldara, col. 4, lines 10-12). Therefore, nowhere does Caldara teach that "a multicast mast entry in said connection table, said multicast mast entry holding address locations at which multicast ATM cells are stored . . . ." Instead, the SAT taught in Caldara points to time slots at which cells are sent out of the TSPP. As indicated by Caldara "[w]hen the pointer is directed toward a slot, the TSPP uses the corresponding entry 51 in the SAT to obtain a cell for launching into the switch fabric 10."

Caldara, therefore, also does not teach "generating one or more multicast member entries associated with said multicast master entry in said connection entry, each multicast member entry identifying a destination connection on which said multicast ATM cells are to be transmitted," as is recited in claim 1, because Caldara does not teach a "multicast master entry."

Further, Caldara et al. does not teach "indicating said multicast master entry inactive according to a comparison between the count field and the limit field," as is recited in claim 1. The Examiner has indicated that the count field and the limit field recited in the claims are fulfilled by the "scoreboard" and the "map" teachings of Caldara. The map of Caldara indicates a list of those cells to be transmitted while the scoreboard serves as a check-off function to indicate that all of the cells have been sent. According to the teachings of Caldara,

> [i]n order to track point-to-multipoint transmission executed at different points in time, the switch includes a map 56 and scoreboard 58, and the SAT 20 includes a three bit subqueue 60 field associated with each slot. The map and scoreboard are each 8 bits long and form bitmasks. The map is initialized according to the subqueues which act as offsets into the map. For example, subqueue "110" indicates an offset of 6 and subqueue "100" indicates an offset of 4. Hence, bits 4 and 6 in the map are initialized to logic "1" and the other bits are initialized to logic "0." The scoreboard is initialized to all logic "0" bits.

(Caldara, col. 5, lines 11-21). Therefore, the map indicates which cells are to be transmitted and is not a "limit" as recited in claim 1. As is further indicated in Caldara,

> [t]racking is realized by updating the scoreboard when copies of cells are transmitted. When the pointer reaches the slot corresponding to the connection for the enqueued point-to-multipoint cell, e.g., "a (4)," the offset indicated by the subqueue (110 indicating 6) is employed to set bit 6 of the scoreboard. The scoreboard is then compared to the map and if a complete match is determined then each cell has been transmitted and the scoreboard is cleared. If the map and scoreboard do not match completely then the point-to-multipoint transmission has not been made to each designated output queue. The updated scoreboard and map thus track which designated output ports have received copies of the cell.

(Caldara, col. 5, lines 22-35). Therefore, the scoreboard checks-off cells that have been sent and is not a "count" as recited in claim 1. The map and the scoreboard, therefore, are not fairly identified with the "limit" and "count" recited in claim 1 of the present application. Therefore, Calbara also does not teach "indicating said multicast master entry inactive according to a comparison between the count field and the limit field," as is recited in claim 1.

Claim 1, then, is allowable over Calbara. Claims 9, 15, and 19 are allowable over Calbara for much the same reasons.

Claim 9, for example, recites "a connection table, said connection table including a multicast master entry and one or more multicast member entries associated with said multicast

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master entry; said multicast mast entry holding address locations at which multicast ATM cells are stored, and including a limit field and a count field; and said one or more multicast member entries identifying a destination connection on which said multicast ATM cells are to be transmitted" which is not taught by Calbara, as was discussed above. Further, claim 9 recites "said limit field and said count field are compared to determine an active status of one of said multicast member entries" as is also not taught by Calbara, as was discussed above. Therefore, claim 9 is allowable for at least the reasons discussed above with respect to claim 1.

Claim 15 recites "a connection table, said connection table including a multicast master entry and one or more multicast member entries associated with said multicast master entry; . . . said multicast master entry holding address locations at which multicast ATM cells are stored, and including a limit field and a count field; and wherein said one or more multicast member entries are linked to each other through a circular double linked list, and said limit field is set to a predefined value and said count field is initialized to a predefined initial value, and said limit field and said count field are compared to determine an active status of one of said multicast member entries." Therefore, claim 15 is allowable over Calbara for reasons discussed above with respect to claim 1.

Claim 19 recites "generating one or more connection entries, each connection entries identifying a destination connection and an output port number on which ATM cells are to be transmitted, each of said connection entry including a limit field and a count field; . . . and comparing a value in said count field with said value in said limit field to determine an active status of the connection entry." Therefore, claim 19 is allowable over Calbara for reasons discussed above with respect to claim 1.

Claim Rejections Under 35 U.S.C. § 103

The Examiner has rejected claims 2-7, 10-13, 16-18, and 20-25 under 35 U.S.C. § 103(a) as

being unpatentable over the combination of Caldara and Holden (U.S. 6, 134, 218). Specifically,

the Examiner rejected claims 2-4, 7, 10-11, 13, 16-17, 20-21, and 23-25 as being unpatentable

over Caldara in view of Holden. The Examiner further rejected claims 5, 6, 12, 18, and 22 as

being unpatentable over Holden in view of Caldara. However, as discussed above, Caldara does

not teach the elements of claims 1, 9, 15, and 19. Holden does not cure the defects in the

teachings of Caldara.

Holden teaches "[a] congestion detection system and method for an advanced ATM

network [which] measures congestion in a number of dimensions." Holden does not teach or

suggest multicasting and therefore aspects of multicasting, such as "a multicast mast entry" or

"one or more multicast member entries" as is recited in claims 1, 9, and 15 or "one or more

connection entries identifying a destination connection and an output port number on which

ATM cells are to be transmitted" as recited in claim 19, are not taught in Holden.

Therefore, claims 2-7, which depend from claim 1, are allowable for at least the same

reasons as is claim 1; Claims 10-13, which depend from claim 9, are allowable for at least the

same reasons as is claim 9; Claims 16-18, which depend from claim 15, are allowable for at least

the same reasons as is claim 15; and Claims 20-25, which depend from claim 19, are allowable

for at least the same reasons as is claim 19.

Allowable Subject Matter

The Examiner has indicated that claims 8 and 14 are objected to "but would be allowable

if rewritten in independent form including all of the limitations of the base claim and any

intervening claims." Accordingly, claims 8 and 14 have been amended to include all of the limitations of the base claim and any intervening claims.
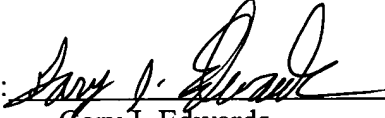
CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: July 13, 2004

By: _Gary J. Edwards_
Gary J. Edwards
Reg. No. 41,008

Attachments: Replacement Sheet 1-12 including Figures 1-6, 7a-7e, and 8a-8c.
Red-lined Sheets illustrating the amendments made to Figures 1-4.

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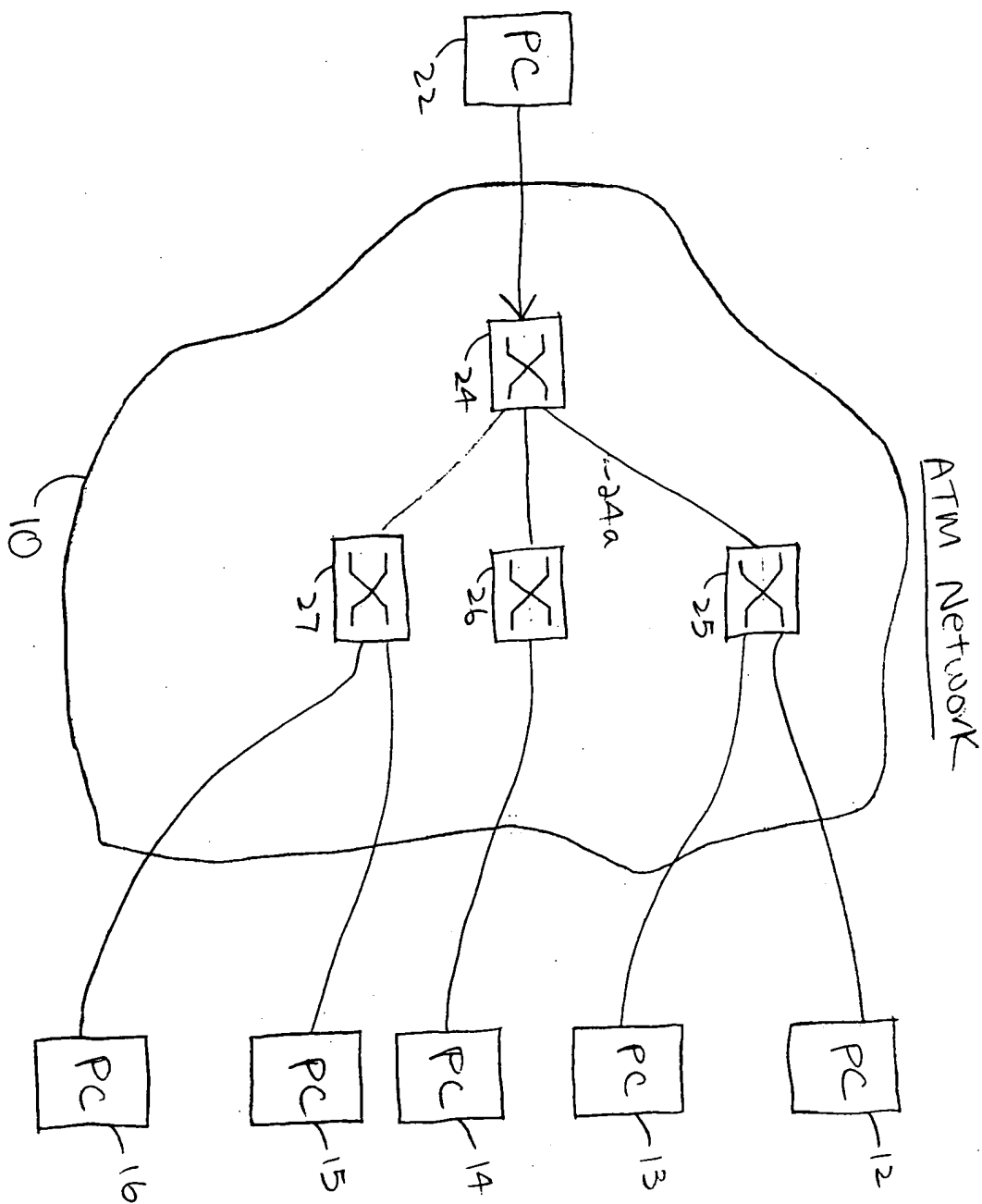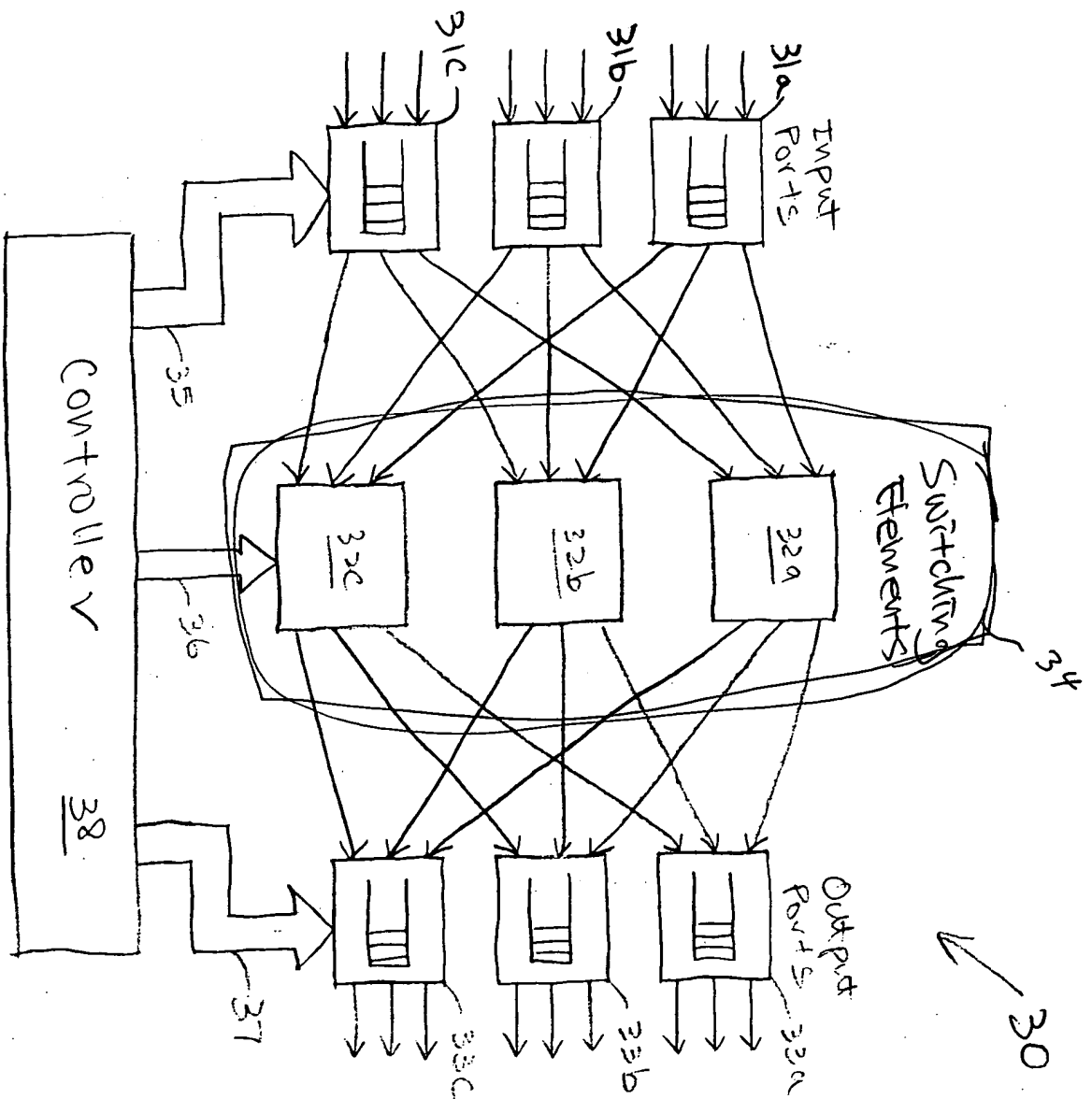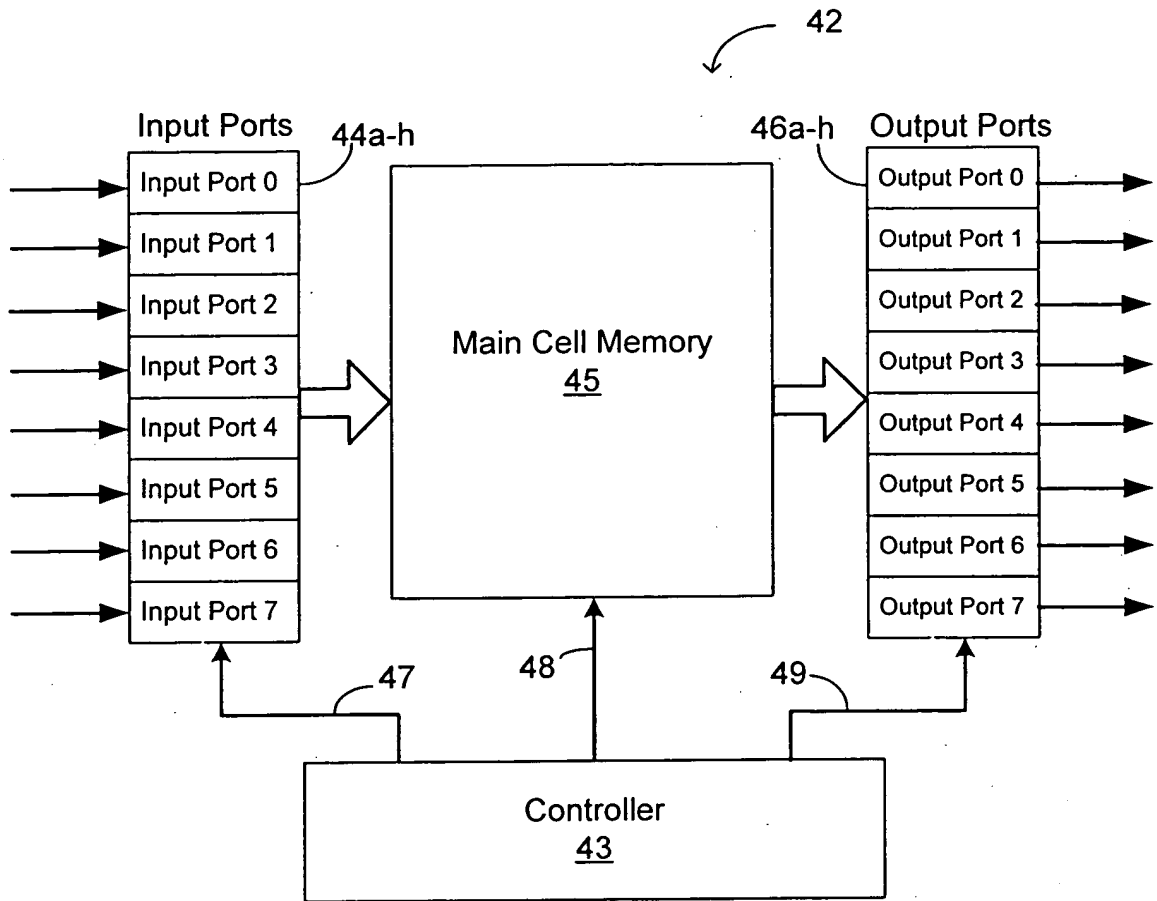
Fig. 1 (Prior Art)

ATM Network

Fig.-2 (prior Art)

Controller 38

Input Ports

31c
31b
31a

35

Switching Elements 34

32c
32b
32a

36

Output Ports

33c
33b
33a

37

30

42

Input Ports 44a-h   46a-h **Output Ports**

Input Ports		Output Ports
Input Port 0		Output Port 0
Input Port 1		Output Port 1
Input Port 2	Main Cell Memory	Output Port 2
Input Port 3	**45**	Output Port 3
Input Port 4		Output Port 4
Input Port 5		Output Port 5
Input Port 6		Output Port 6
Input Port 7		Output Port 7

47   48   49

Controller
43

Figure 3 (Prior Art)

VC Memory

Multicast Group

DVPI	DVCI						
DVPI	DVCI	0001 0000	...		+	T	C
DVPI	DVCI	1001 1111	...		+	T	C
DVPI	DVCI	Output Port #	...				
DVPI	DVCI	Output Port #	...				
DVPI	DVCI	Output Port #	...				

Fig. 4 (prior Art)